Detector Support Group

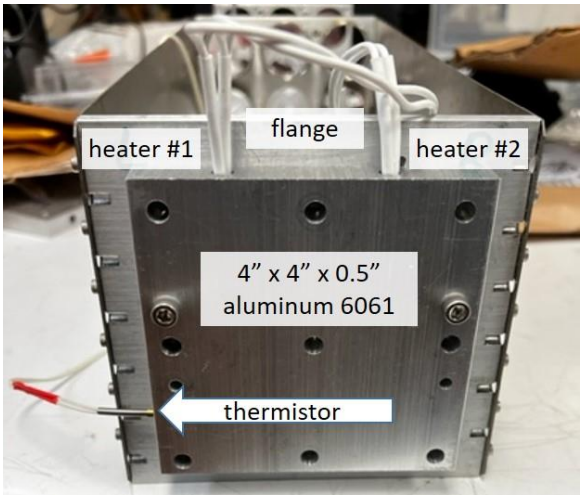
We choose to do these things "not because they are easy, but because they are hard".

Weekly Report, 2023-03-08

Hall A – ECAL

Brian Eng and Marc McMullen

- Disassembled test stand and removed the silicon heater from the supermodule to check condition
  - ✶ The silicon had no delamination and the supermodule was undamaged
- Wrote LabVIEW code to control the heater ramp rate
- Prototyping heaters using two 24-V, 70-W cartridge heaters in a 4" x 4" x 0.5" aluminum plate
  - ✶ Ordered components
  - ✶ Machined aluminum plate and installed two heaters and one thermistor
  - ✶ Rewired test stand to use two channels to supply voltage (one for each heater)



Hall A – GEp

Mindy Leffel

- Terminated two high voltage, Fischer, 27-pin connectors

Hall A – Møller

Mary Ann Antonioli and Brian Eng

- Began Illustrator diagram for Phoebus screen for magnet #2 temperatures
  - ✶ The Phoebus diagram based on AutoCAD drawing coordinates has lines that don't line up correctly
- Installed trial version of Siemens PLC software suite TIA Portal v18 (Totally Integrated Automation); still no word on missing licenses ordered
- Siemens distributor updated parts delivery dates; some items have been changed to 2024
- Reviewed drafts of RTD drawings Kaiyi put on document control

Hall A – SoLID

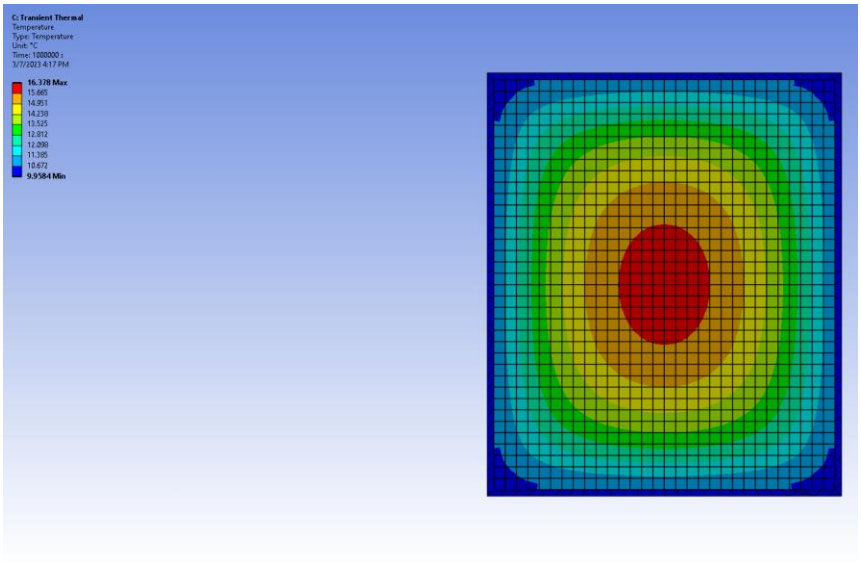
Pablo Campero

- Completed requested changes to *Solenoid Cooldown* and *Solenoid Neck Temperatures* HMI screens

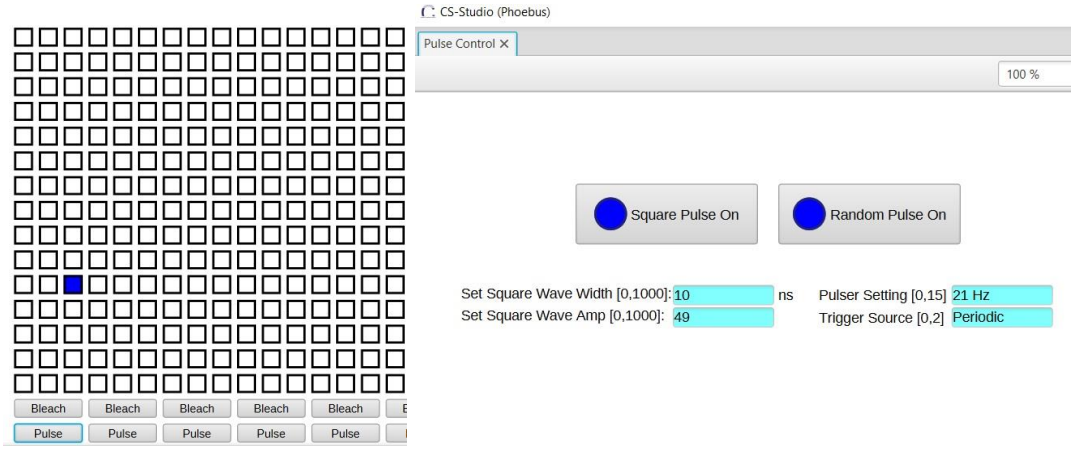
Hall C – NPS

Mary Ann Antonioli, Peter Bonneau, Aaron Brown, Pablo Campero, Brian Eng, Mindy Leffel, and Marc McMullen

- Ran Ansys Transient Thermal simulation of crystal array with dividers (carbon fiber and mu-metal) and copper cooling shell
  - ✶ Q = 0.3 W
  - ✶ Film coefficient: 5 W/m^2°C
  - ✶ Ambient: 20–22°C
  - ✶ Copper shell temp: 10°C
  - ✶ Max temperature after 1E6 s (277.77 hrs): 16.378°C



- Continued developing Python script for Keysight extension cable testing
  - ✶ Included a timestamp after each temperature and voltage measurement
  - ✶ Wrote test procedure
- Wrote Python code to generate a new version of the VLD Control GUI
  - ✶ Made a prototype screen to verify that Boolean widgets can access a single bit from a PV; can directly use PVs for channel masks to enable or disable channels
  - ✶ Adding PVs
  - ✶ Adding bleach mode and pulse mode settings and readback



- Added channel status byte monitor to the high voltage channels pop-up screen
- Evaluating implementation of alarm arrays within the Phoebus test system EPICS softIOC
- Terminated one 50-conductor, D-sub connector cable; 12 of 12 completed

Hall D – JEF

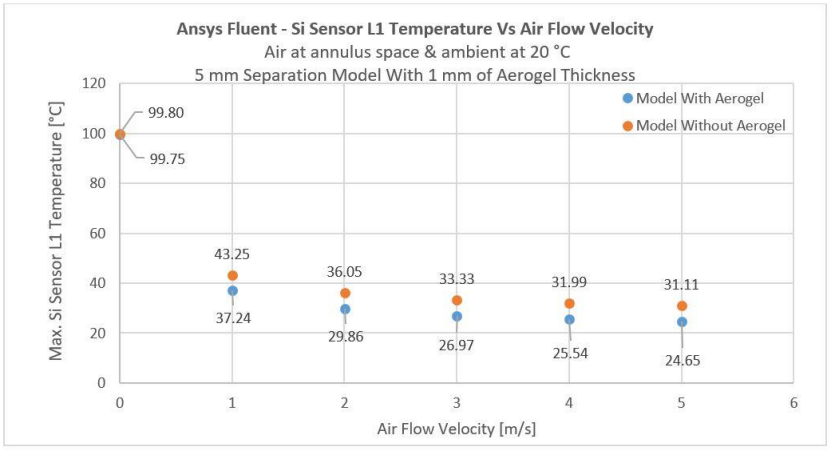
Mindy Leffel

- Populated 120 PMT bases

EIC

Brian Eng, Pablo Campero, and Marc McMullen

- Disassembled the thermal test stand
- Researched and ordered aerogel for insulating the thermal test stand
- Ran thermal simulation for model with 5 mm of separation between beampipe and silicon, with 1 mm and 0.5 mm of aerogel insulator and without insulator, and air flow through the annulus space and enclosure at 3 and 4 m/s
    - ✶ Plotted results of silicon temperature vs velocity, with 1-mm thick aerogel and without

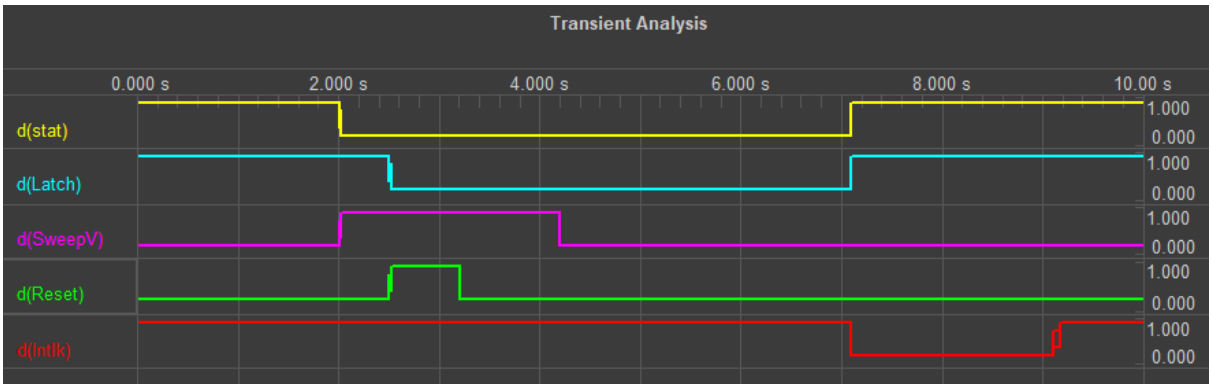


- Completed 3D model of beampipe used in test stand

EIC-DIRC

Tyler Lemon and Marc McMullen

- Reviewed interlock schematic
- Compiled list of items to procure for laser test area
- Investigating circuit for photodiode readout and the use of an op-amp in a transimpedance amplifier
- Designed 60" x 18" x 0.063" aluminum panels for optical table sidewalls
    - ✶ Panels will be machined and powder coated in matte black by vendor
- Simulated laser interlock circuit in Altium with circuit inputs replaced by programmable voltage sources
    - ✶ Interlock status and latched status monitored using digital probes
    - ✶ Results plotted on timing graph show where the inputs were toggled and the circuit's response



DSG Website

Peter Bonneau

- Revised the main DSG website page and added additional content